Amendments to the Claims:

1-21. (Cancelled)

22. (New) A lead frame comprising:

a frame;

a chip mounting board disposed within the frame and including a plurality of openings disposed and arranged therein in a manner defining a peripheral portion which includes:

a generally planar first peripheral surface;

a generally planar second peripheral surface disposed in opposed relation to the first peripheral surface; and

a plurality of third peripheral surfaces formed between the first and second peripheral surfaces in opposed relation to the first peripheral surface;

a plurality of tie bars connected to and extending between the frame and the chip mounting board for supporting the chip mounting board within the frame; and

a plurality of leads connected to the frame and extending about the periphery of the chip mounting board in spaced relation thereto.

23. (New) The lead frame of Claim 22 wherein the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines:

a generally planar first central surface;

a generally planar second central surface disposed in opposed relation to the first central surface; and

a third central surface formed between the first and second central surfaces in opposed relation to the first central surface, the third central surface circumventing the second central surface.

24. (New) The lead frame of Claim 23 wherein each of the tie bars defines:

a generally planar first tie bar surface;

a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and

a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the chip mounting board.

25. (New) The lead frame of Claim 23 wherein each of the leads defines:

a generally planar first lead surface;

a generally planar second lead surface disposed in opposed relation to the first lead surface; and

a third lead surface formed between the first and second lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the chip mounting board than the second lead surface.

26. (New) The lead frame of Claim 22 wherein each of the openings comprises an elongate slot.

27. (New) The lead frame of Claim 22 wherein each of the openings comprises a hole.

28. (New) The lead frame of Claim 23 wherein:

the peripheral portion of the chip mounting board has a generally square configuration defining four segments; and

the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals.

29. (New) The lead frame of Claim 28 wherein:

the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments;

the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and

the leads are segregated into four sets which extend toward respective ones of the segments of the peripheral portion.

30. (New) A semiconductor package comprising:

a lead frame comprising:

a frame;

a chip mounting board disposed within the frame and including a plurality of openings disposed and arranged therein in a manner defining a peripheral portion which includes:

a generally planar first peripheral surface;

a generally planar second peripheral surface disposed in opposed relation to the first peripheral surface; and

a plurality of third peripheral surfaces formed between the first and second peripheral surfaces in opposed relation to the first peripheral surface;

a plurality of tie bars connected to and extending between the frame and the chip mounting board for supporting the chip mounting board within the frame;

a plurality of leads connected to the frame and extending about the periphery of the chip mounting board in spaced relation thereto;

a semiconductor chip attached to the chip mounting board and including a plurality of input-output pads;

at least two conductive wires mechanically and electrically connecting respective ones of the input-output pads of the semiconductor chip to respective ones of the peripheral portion of the chip mounting board and the leads; and

a sealing part for sealing the chip mounting board, the tie bars, the leads, the semiconductor chip and the conductive wires, the sealing part being configured such that the second surface of the peripheral portion is exposed therein.

31. (New) The semiconductor package of Claim 30 wherein the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines:

a generally planar first central surface;

a generally planar second central surface disposed in opposed relation to the first central surface; and

a third central surface formed between the first and second central surfaces in opposed relation to the first central surface, the third central surface circumventing the second central surface;

the semiconductor chip being attached to the first central surface of the chip mounting board.

32. (New) The semiconductor package of Claim 31 wherein each of the tie bars defines:

a generally planar first tie bar surface;

a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and

a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the chip mounting board.

33. (New) The semiconductor package of Claim 32 wherein each of the leads defines:

a generally planar first lead surface;

a generally planar second lead surface disposed in opposed relation to the first lead surface; and

a third lead surface formed between the first and second third lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the chip mounting board than the second lead surface.

34. (New) The semiconductor package of Claim 33 wherein the sealing part is configured such that the second central surface of the central portion of the chip mounting board, the second peripheral surface of the peripheral portion of the chip mounting board, the second tie bar surface of each of the tie bars, and the second lead surface of each of the leads are exposed therein.

35. (New) The semiconductor package of Claim 31 wherein the semiconductor chip is attached to the first central surface via an adhesive layer.

36. (New) The semiconductor package of Claim 30 wherein the conductive wire is connected to a portion of the first peripheral surface of the chip mounting board which is not disposed in opposed relation to any of the third peripheral surfaces.

37. (New) The semiconductor package of Claim 30 wherein:

the peripheral portion of the chip mounting pad has a generally square configuration defining four segments; and

the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals.

38. (New) The semiconductor package of Claim 37 wherein:

the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments;

the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and

the leads are segregated into four sets which extend toward respective ones of the segments of the peripheral portion.

39. (New) A semiconductor package comprising:

a lead frame comprising:

a chip mounting board including a plurality of openings disposed and arranged therein in a manner defining a peripheral portion which includes:

a generally planar first peripheral surface;

a generally planar second peripheral surface disposed in opposed relation to the first peripheral surface; and

a plurality of third peripheral surfaces formed between the first and second peripheral surfaces in opposed relation to the first peripheral surface; and

a plurality of leads extending about the periphery of the chip mounting board in spaced relation thereto;

a semiconductor chip attached to the chip mounting board and electrically connected to at least one of the leads; and

a sealing part at least partially covering the chip mounting board, the leads, and the semiconductor chip such that the second surface of the peripheral portion is exposed therein.

40. (New) The semiconductor package of Claim 39 wherein:

the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines opposed, generally planar first and second central surfaces;

each of the leads defines opposed, generally planar first and second lead surfaces; and

the sealing part is configured such that the second central surface of the central portion of the chip mounting board, the second peripheral surface of the peripheral portion of the chip mounting board, and the second lead surface of each of the leads are exposed therein.

41. (New) The semiconductor package of Claim 39 wherein:

the peripheral portion of the chip mounting board has a generally square configuration defining four segments; and

the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals.

42. . (New) The semiconductor package of Claim 41 wherein:

the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments;

the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and

the leads are segregated into four sets which extend toward respective ones of the segments of the peripheral portion.